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Improving performance of synapse processing in massively parallel neuromorphic systems

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Supervisor: Dr David R. Lester
APT group

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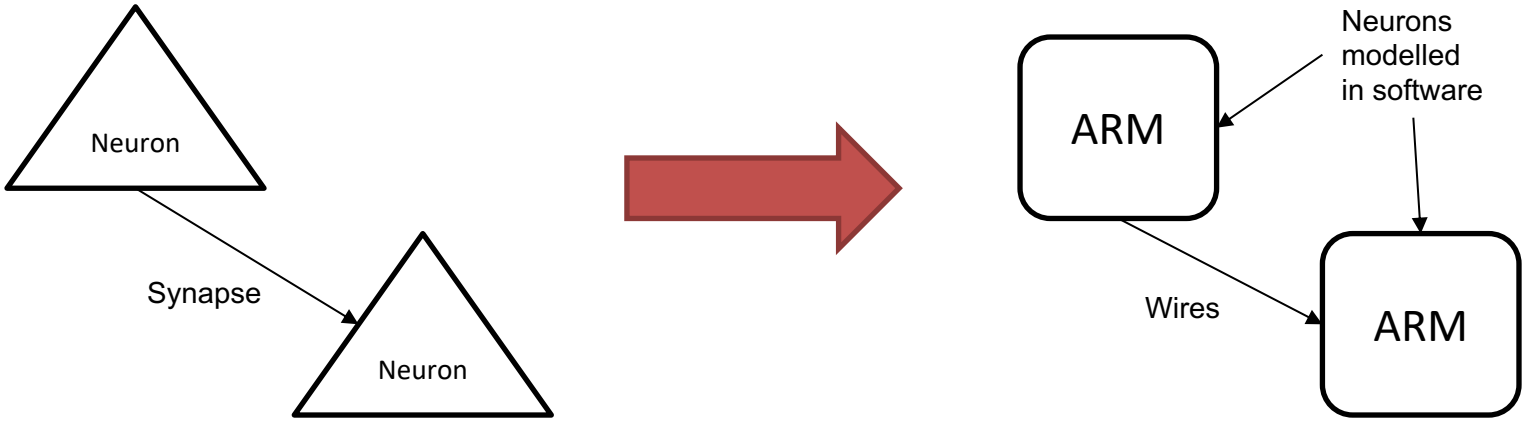
SpiNNaker Neuromorphic Computer

- Neuromorphic – resembling brain interconnect



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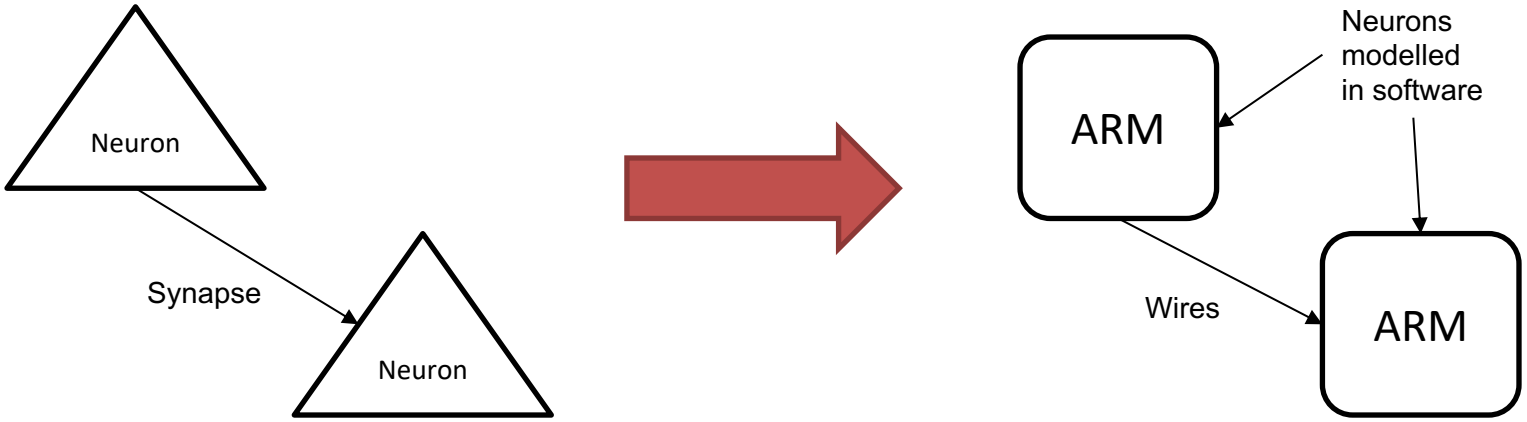

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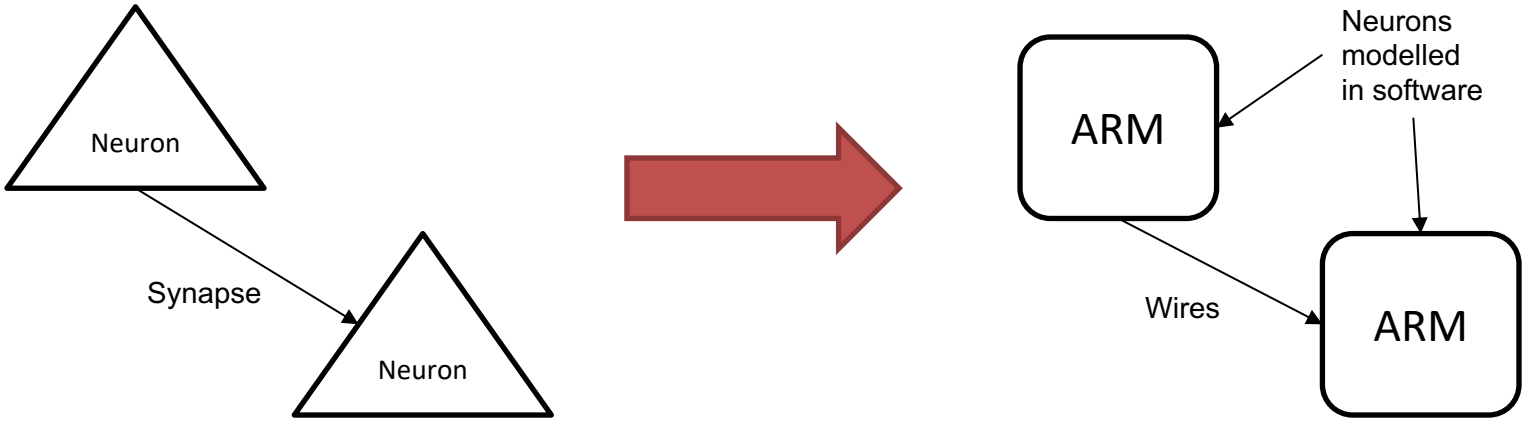
- Main goal: Simulate 1% of human brain.



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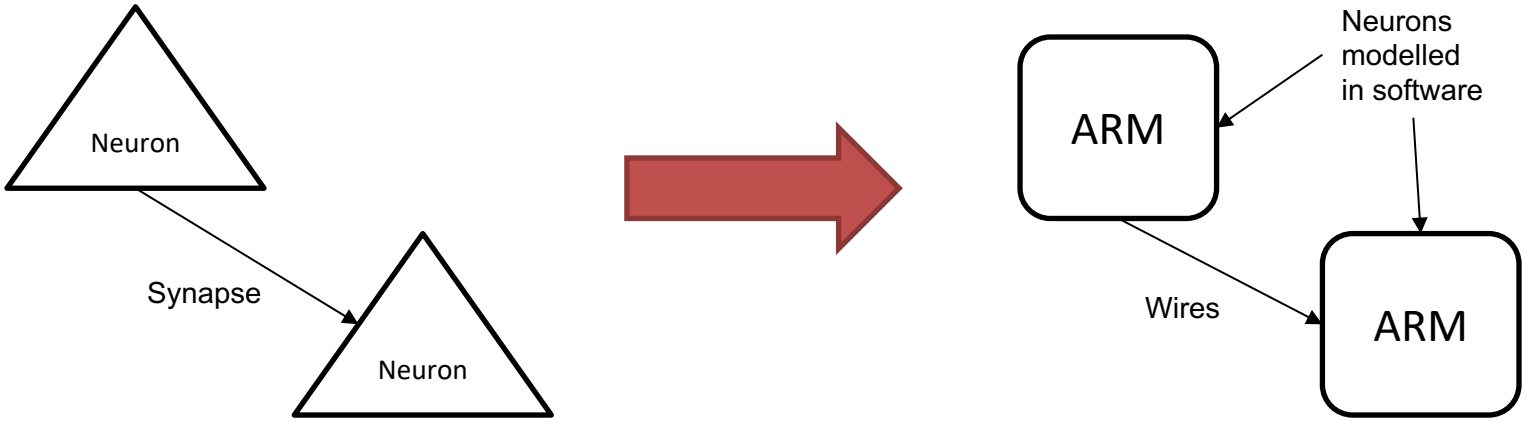
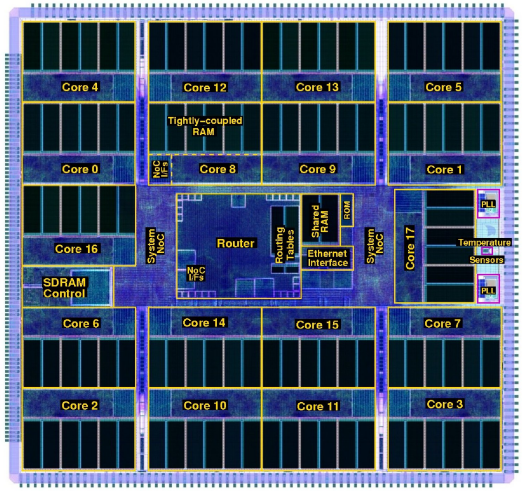
- Main goal: Simulate 1% of human brain.
- Made of ARM cores (Same cores that are in mobile phones)

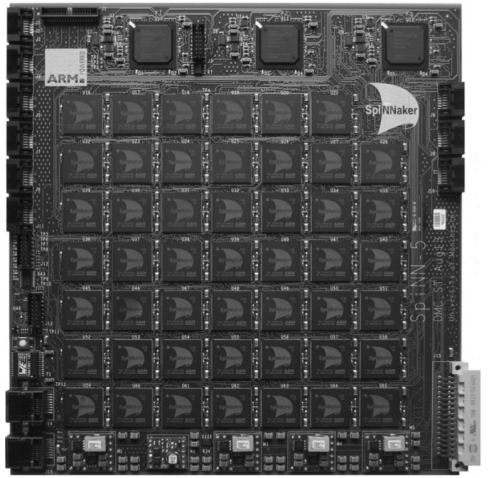


SpiNNaker Neuromorphic Computer

~4000 neurons



SpiNNaker chip



A board with 48 chips

720 boards (1200 boards in final stage for 1% of brain)

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Main challenges of the SpiNNaker project

Hardware:

- Processing millions of signals through million cores
- Power efficiency

Software:

- Biological plausibility – does it simulate accurate brain behavior?
- Real-Time running constraint – can ARM cores run simulation in real-time (Not slowed down).

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What I intend to address in my PhD

Most of the time SpiNNaker spends on processing synapses.

If an algorithm is **learning**, synapse strengths are changed which poses even more challenge.

I am interested in improving this using hardware and software optimizations in order to simulate **larger** neural networks in **real-time**.

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Learning on SpiNNaker-1

- Learning in brain is called **synaptic plasticity**.

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- On SpiNNaker, a mathematical learning rule can be injected to describe synaptic change.

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Learning on SpiNNaker-1

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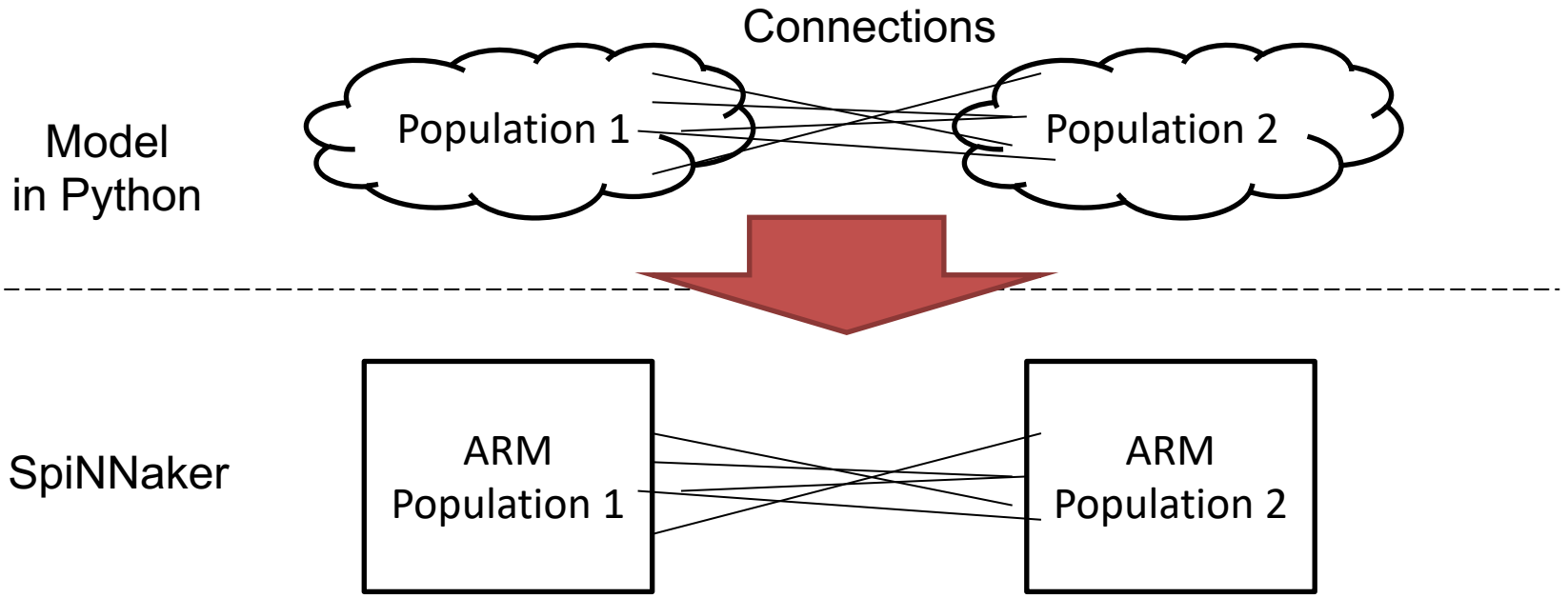
- Strengths of synapses are changing so that some **neurons learn to fire a signal (spike) more often or less often**.
- On SpiNNaker, a mathematical learning rule can be injected to describe synaptic change.
- Most rules involve analyzing a **history of spikes of two neurons connected by a synapse** – slow, memory-heavy process.

Simulating plastic neural networks on SpiNNker

- Each ARM core gets assigned a set (of some controlled size) of neurons that it is responsible for.
- When one neuron spikes, ARM core has to receive or send out a spike.



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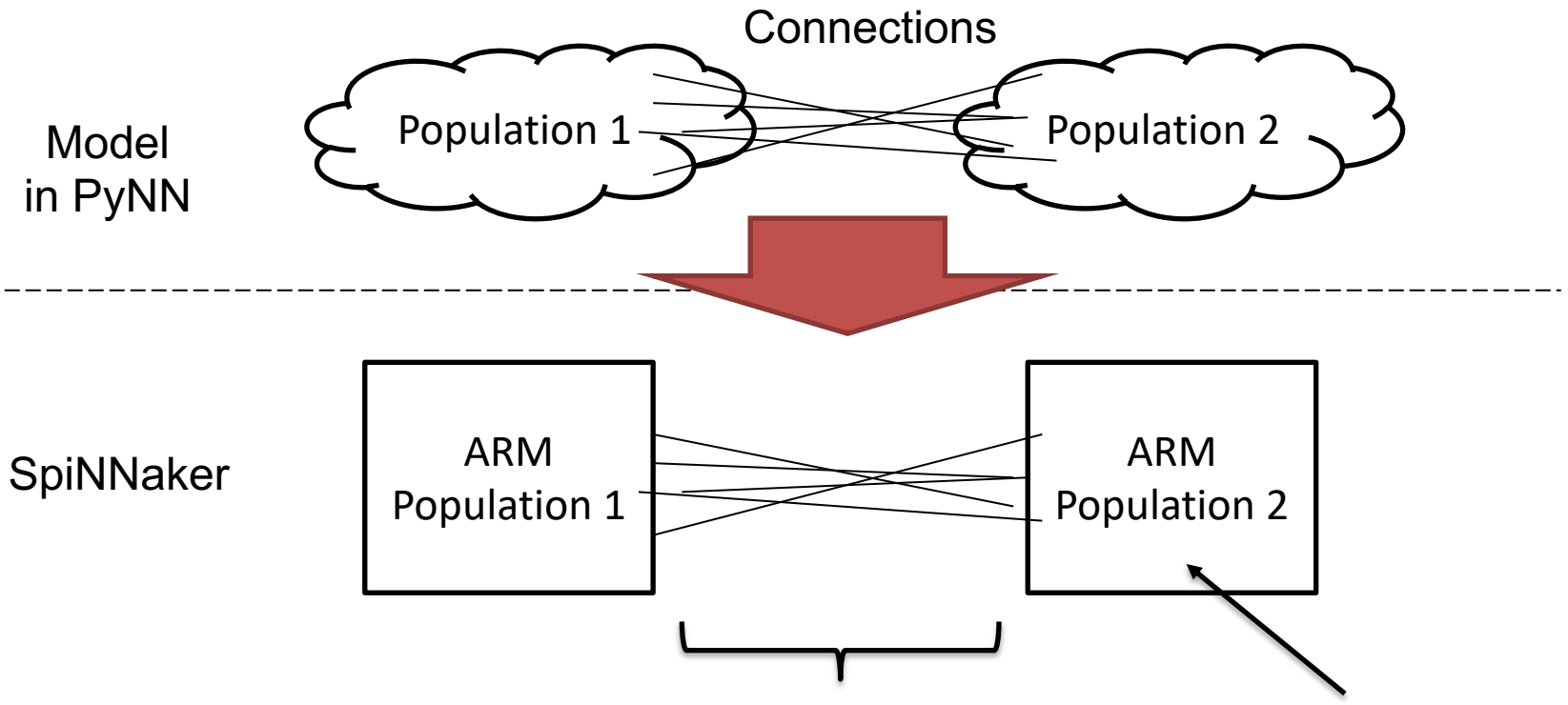
Simulating plastic neural networks on SpiNNker



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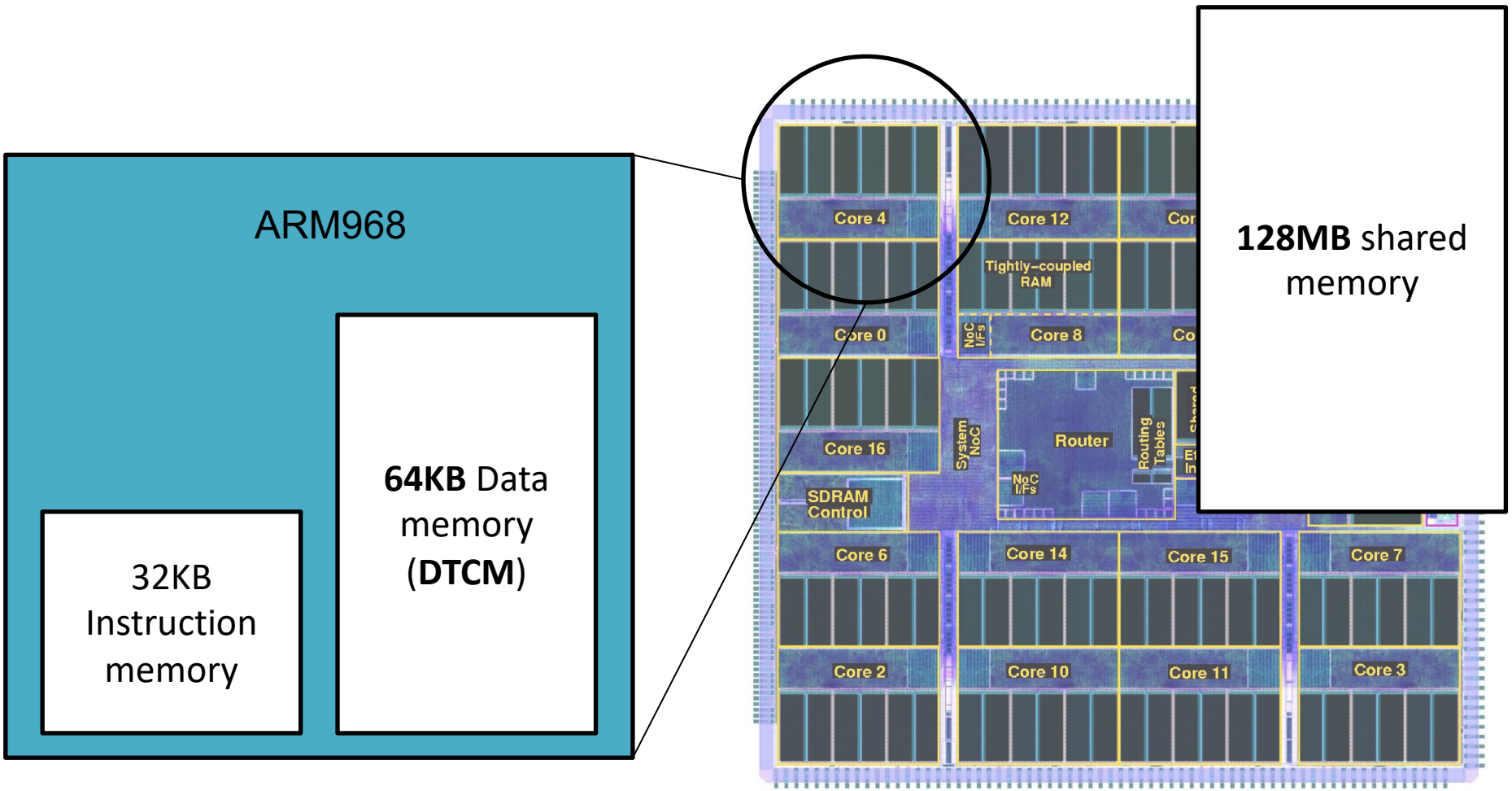
SpiNNaker-1 Chip Tear-Down



Single chip: 18 ARM968 cores and 128MB shared SDRAM

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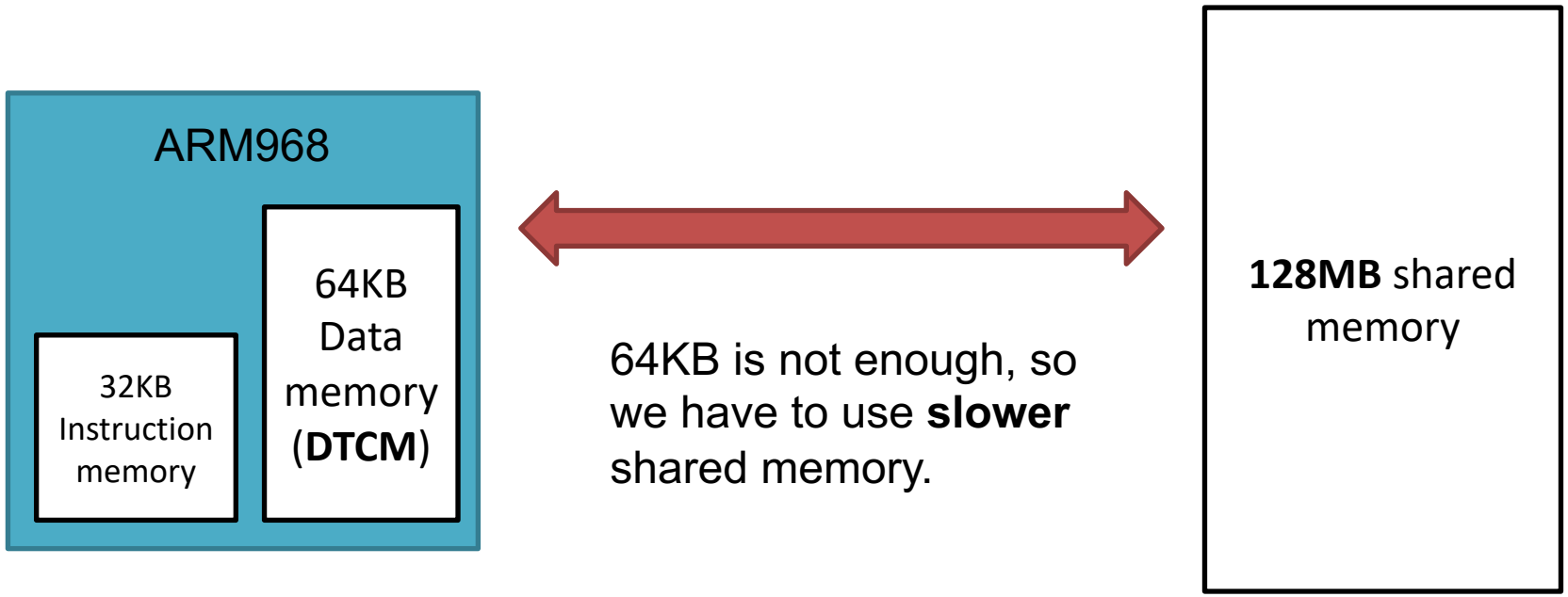

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What ARM core spends time on when receiving a spike

- **Copying** neuron spike history from SDRAM to internal memory.

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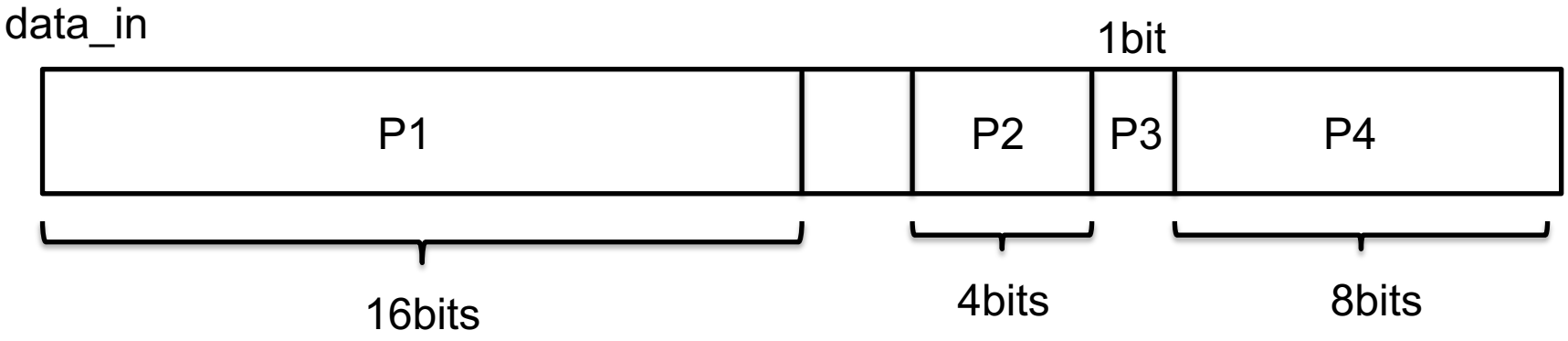
Running example – bit shifting and masking



P1 = (data_in &0xFFFF0000) >> 16
P2 = (data_in & 0x00001E00) >> 9
P3 = (data_in & 0x00000100) >> 8
P4 = (data_in & 0x000000FF)

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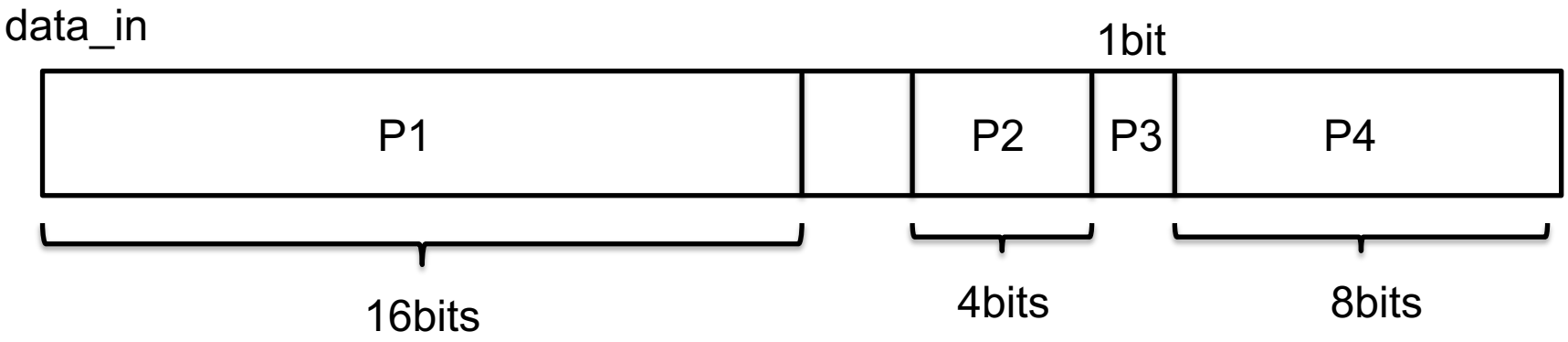

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This is done hundreds of times per 1ms.

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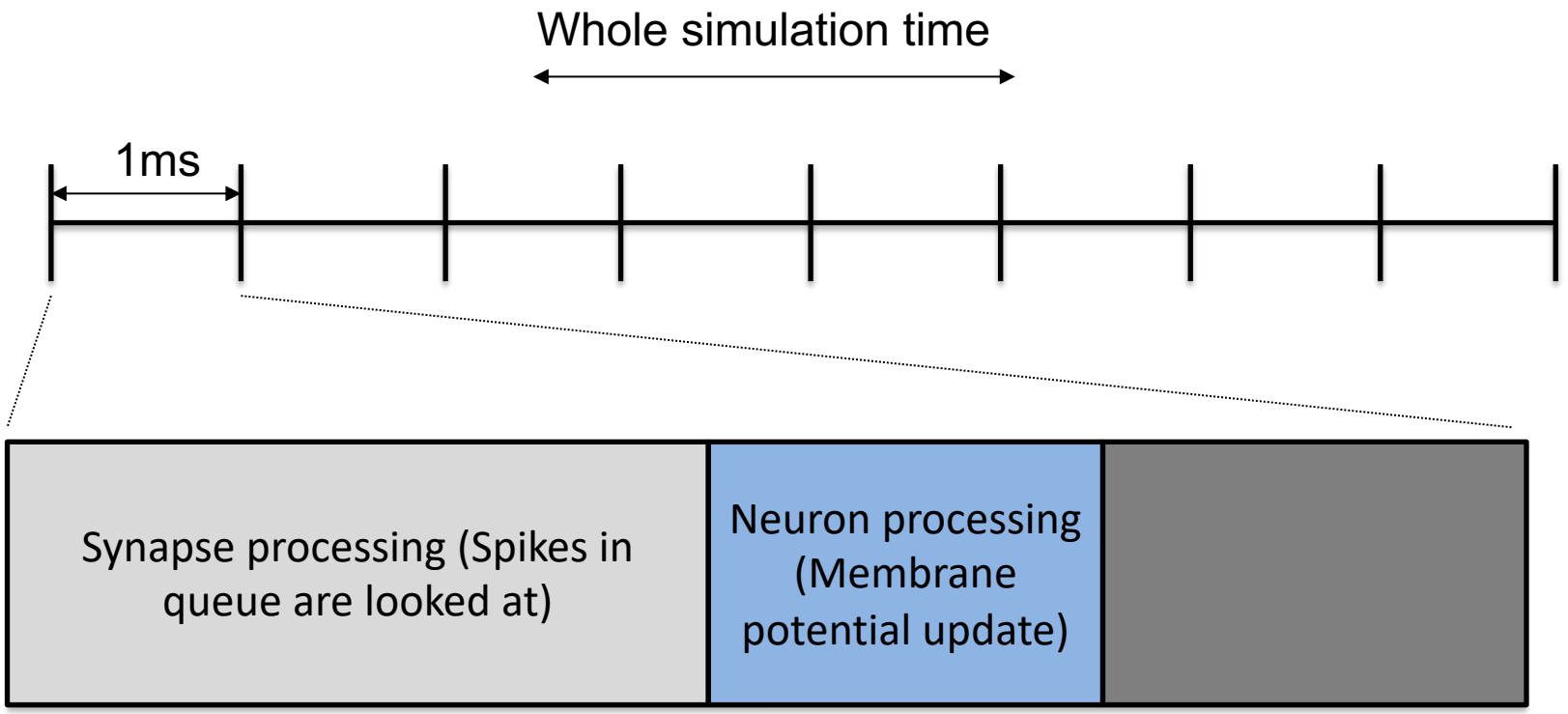
Real-Time simulation constraint



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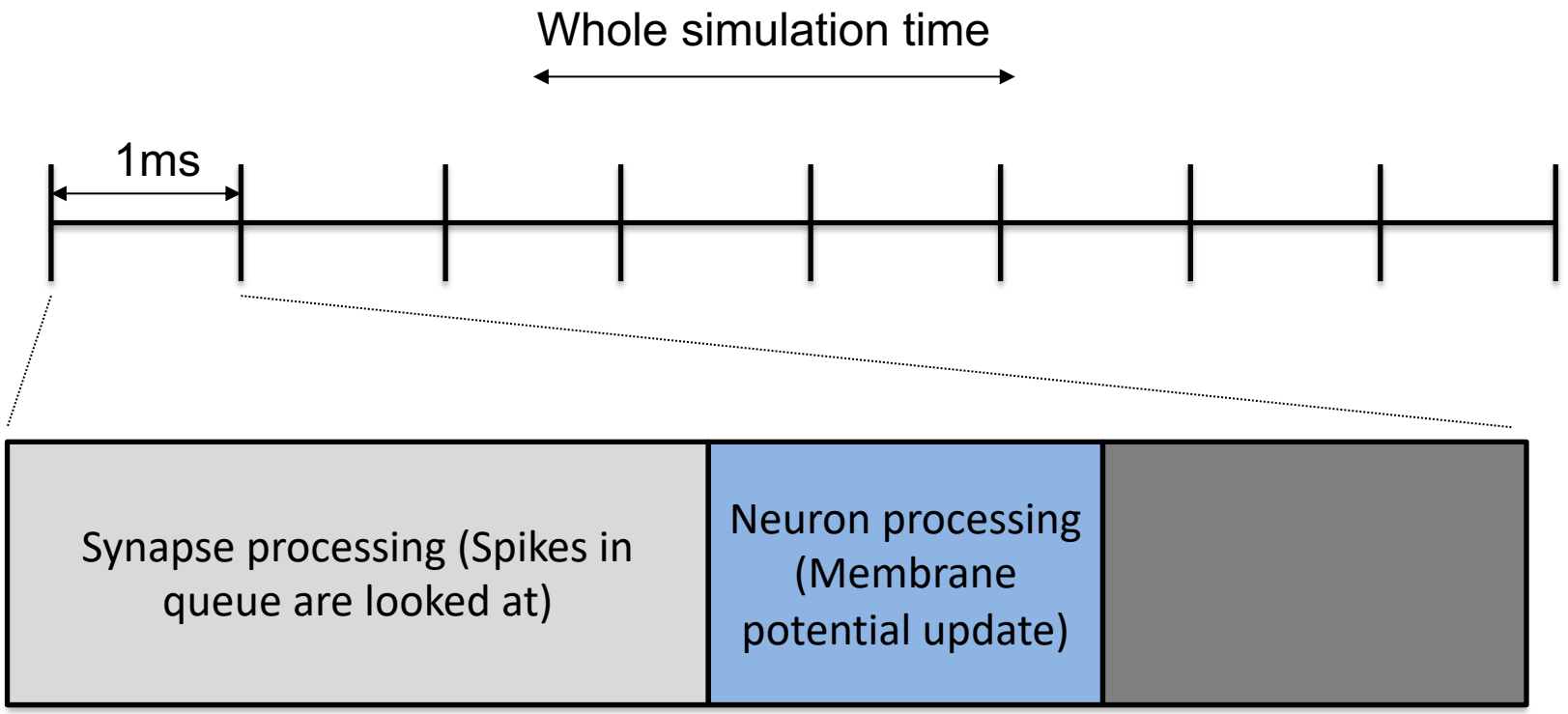

Important rule: Run-time of synapse processing and neuron processing functions combined, cannot overrun 1ms.

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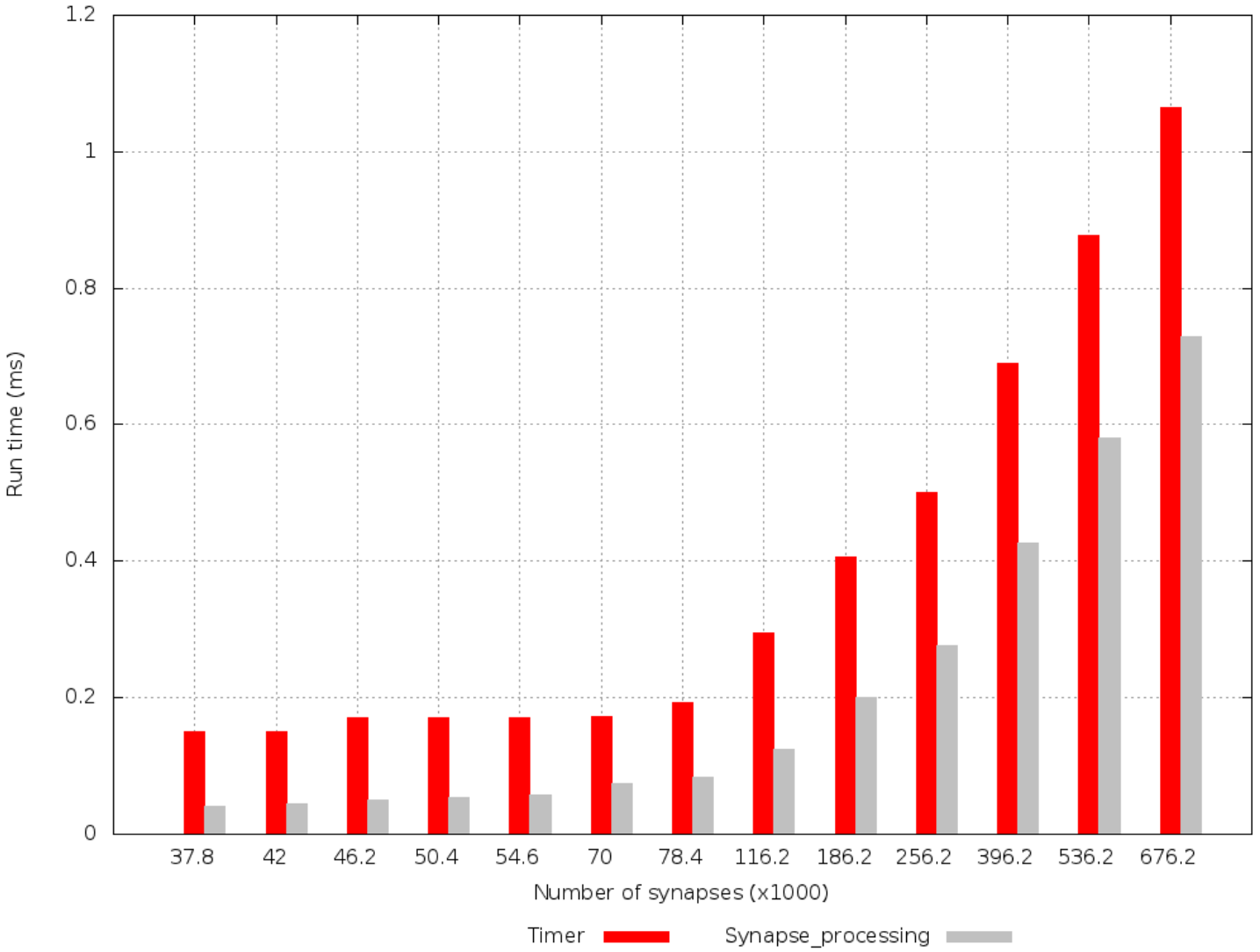

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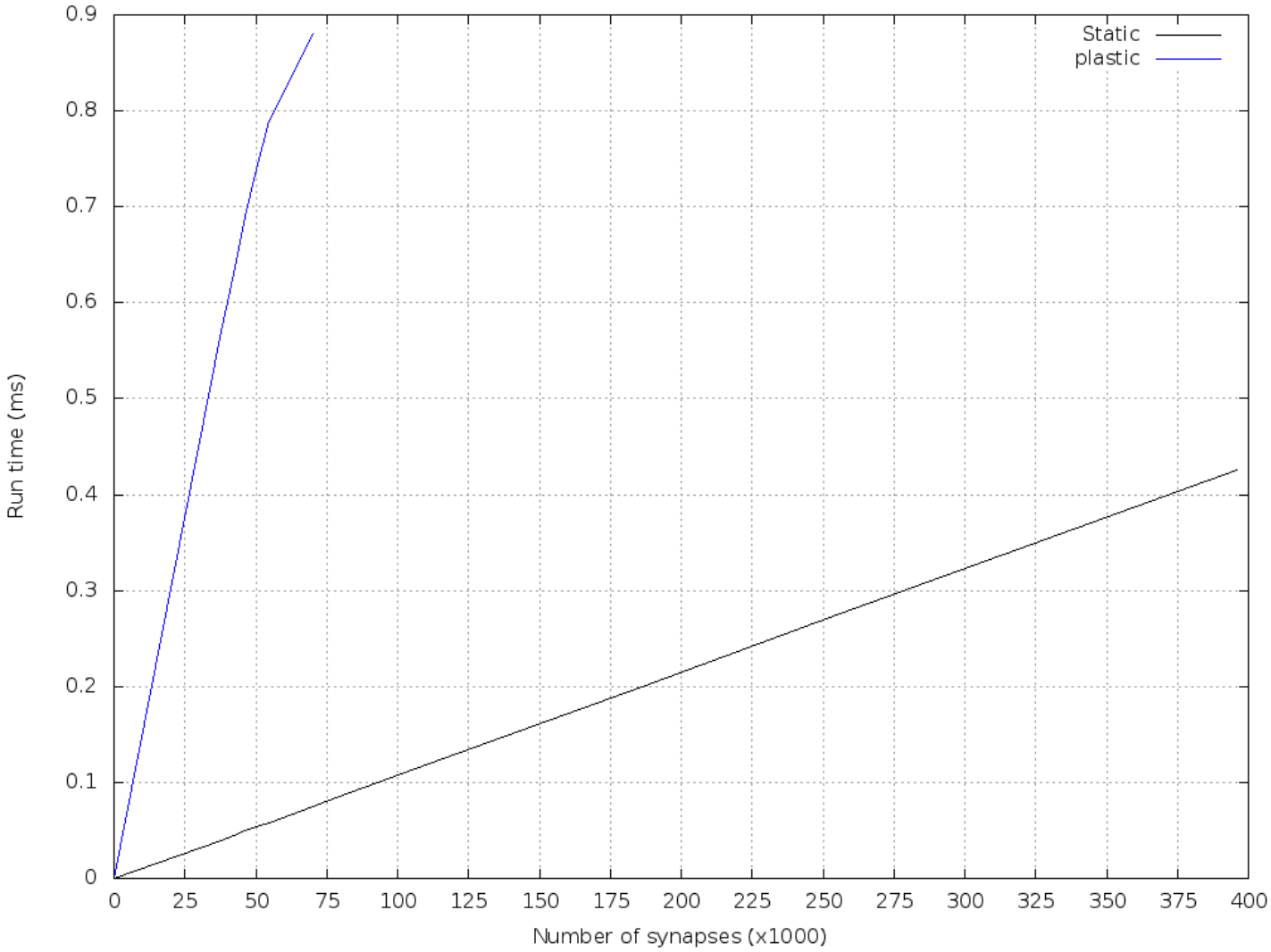

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Methods – Hardware accelerators

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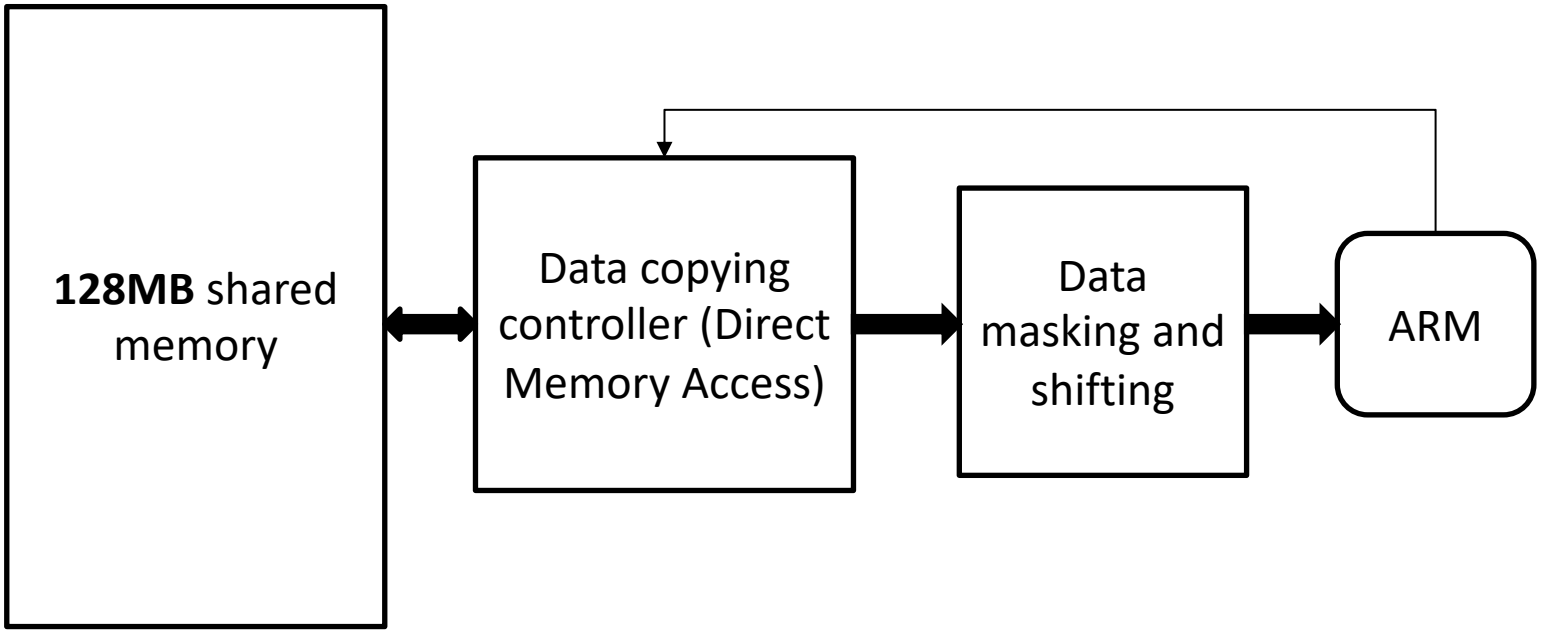
Methods – Hardware accelerators

- Create a hardware module that will do bit-masking and shifting of data before it is written to ARM core.



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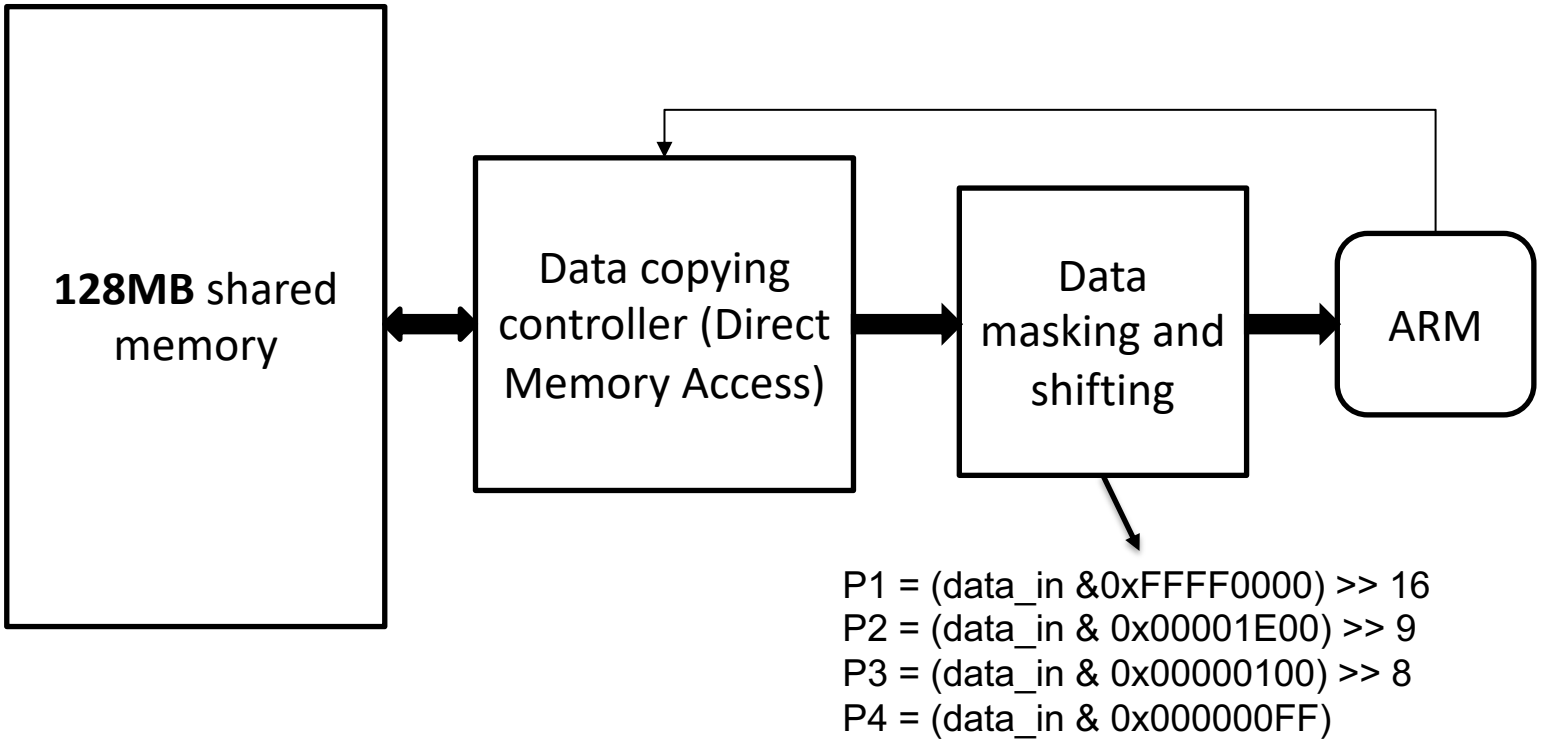

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- Currently all this is done **in software**.
- Create a hardware module that will do EXP and LOG functions **without multiplication** (Using shifting and adding instead).
- More possibilities exist, depending on specific problems of **types of simulations**.
- The main rule is that hardware is fixed, so we have to **identify fixed parts of current and future simulation types**.

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Summary

- Synapse processing on SpiNNaker poses challenges for real-time simulations
- Software optimizations are not enough
- Proposal is to introduce hardware accelerators to speed up the process